

Fig. 1a

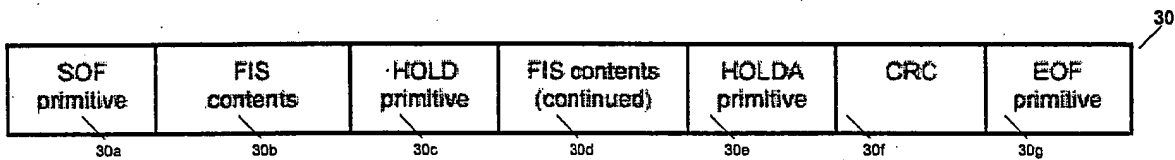


Fig. 1b

				31add		Register access operation		
CS 0 Active		A2	A1	A0	Read		Write	
		0	0	0	Data Port 31dn			
		0	0	1	Error 31e		Features 31f	
		0	1	0	Sector Count [15:8], [7:0] 31sc			
		0	1	1	Sector Number [31:24], [7:0] 31sn			
		1	0	0	Cylinder Low [39:32], [15:8] 31cl			
		1	0	1	Cylinder High [47:40], [23:16] 31ch			
		1	1	0	Device / Head		31dev	
		1	1	1	Status 31s		Command 31c	
CS 1 active		1	1	0	Alternate Status 31as		Device Control 31dc	

Fig. 1c

0	Features	Command	C	R	R	Reserved (0)	FIS Type (27h)	40(i)
1	Dev / Head	Cyl High				Cyl Low	Sector Number	
2	Features (exp)	Cyl High (exp)				Cyl Low (exp)	Sector Num (exp)	
3	Control	Reserved (0)				Sector Count (exp)	Sector Count	
4	Reserved (0)	Reserved (0)				Reserved (0)	Reserved (0)	

Fig. 1d(i) Register FIS Host to Device

0	Error	Status	R	I	R	Reserved (0)	FIS Type (34h)	40(ii)
1	Dev / Head	Cyl High				Cyl Low	Sector Number	
2	Reserved (0)	Cyl High (exp)				Cyl Low (exp)	Sector Num (exp) (0)	
3	Reserved (0)	Reserved (0)				Sector Count (exp)	Sector Count	
4	Reserved (0)	Reserved (0)				Reserved (0)	Reserved (0)	

Fig. 1d(ii) Register FIS Device to Host

0	Reserved (0)	Reserved (0)	R	R	R	Reserved (0)	FIS Type (39h)	40(iii)
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Fig. 1d(iii) DMA Activate FIS, Device to Host

0	Reserved (0)	Reserved (0)	A	I	D	Reserved (0)	FIS Type (41h)	40(vi)
1	0						TAG	
2	0							
3	Reserved (0)							
4	DMA Buffer Offset							
5	DMA Transfer Count							
6	Reserved (0)							

Fig. 1d(iv) DMA Setup FIS

0	Error	R	Status Hi	R	Status Lo	R	I	R	Reserved (0)	FIS Type (A1h)	40(v)
1	SActive 31:0 41										

Fig. 1d(v) Set Device Bits FIS

0	Error	Status	R	I	D	Reserved (0)	FIS Type (5Fh)	40(vi)
1	Dev / Head	Cyl High	Cyl Low			Sector Number		
2	Reserved (0)	Cyl High (exp)	Cyl Low (exp)			Sector Num (exp) (0)		
3	E_Status	Reserved (0)	Sector Count (exp)			Sector Count		
4	Reserved (0)					Transfer Count		

Fig. 1d (vi) PIO Setup FIS

0	Reserved (0)	Reserved (0)	R	R	R	Reserved (0)	FIS Type (46h)	40(vii)
...	N Dwords of data (minimum of one Dword - maximum of 2048 Dwords)							
...								
n								

Fig. 1d (vii) Data FIS

0	Reserved (0)	Pattern Definition	R	R	R	Reserved (0)	FIS Type (58h)	40(viii)
		T A S L F P R V						
1	Data [31:24]	Data [23:16]	Data [15:8]			Data [7:0]		
2	Data [31:24]	Data [23:16]	Data [15:8]			Data [7:0]		

Fig. 1d(viii) BIST Activate FIS

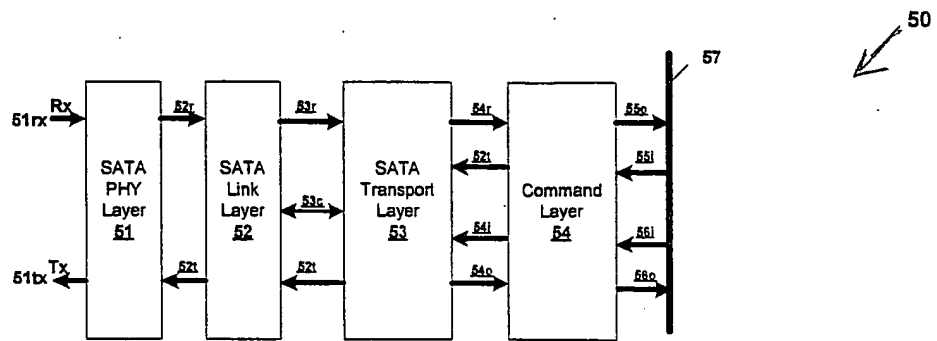


Fig. 2a

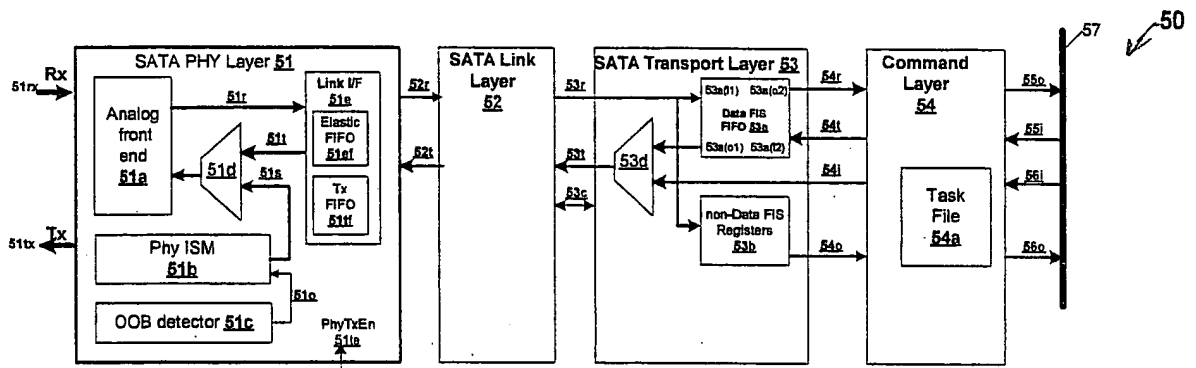


Fig. 2b

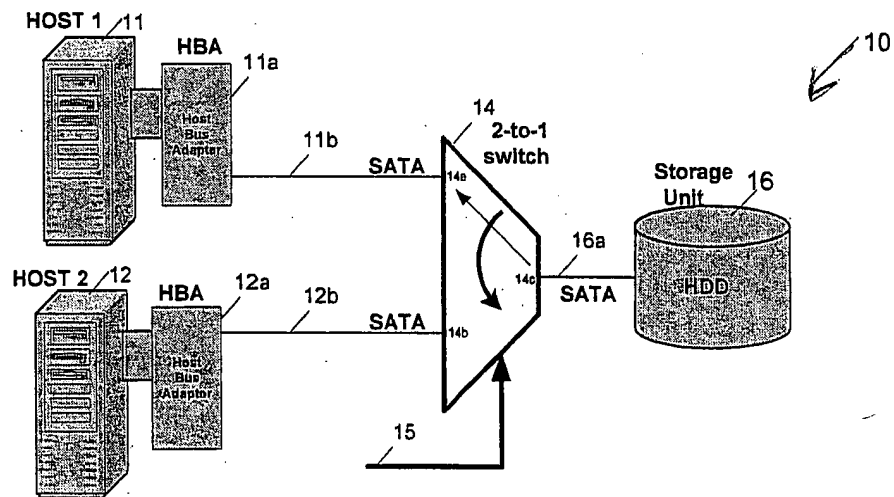


Fig. 3a

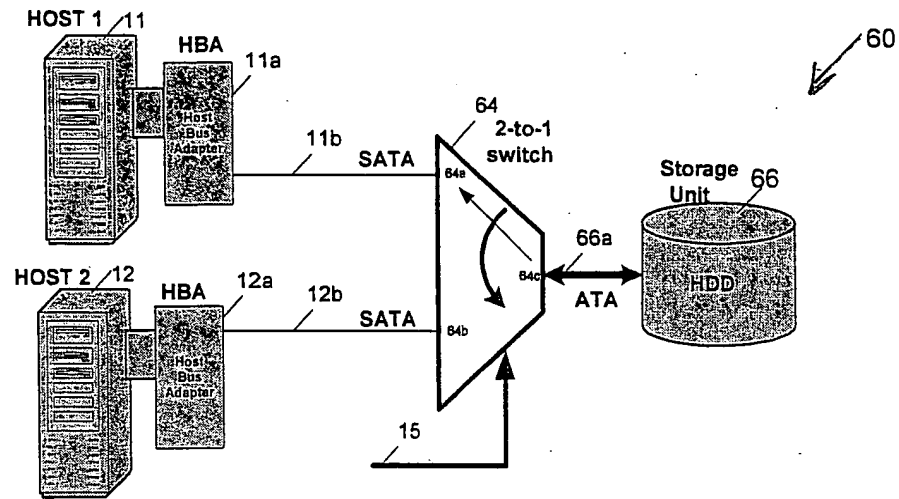


Fig. 3b

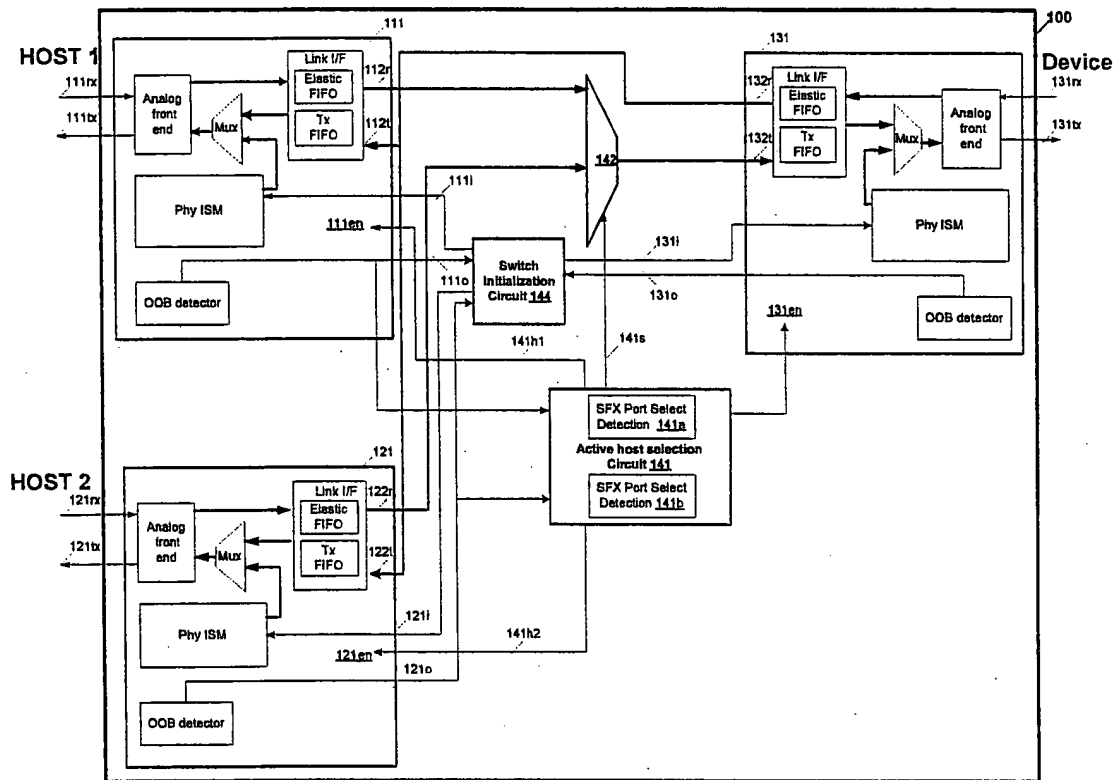


Fig. 4

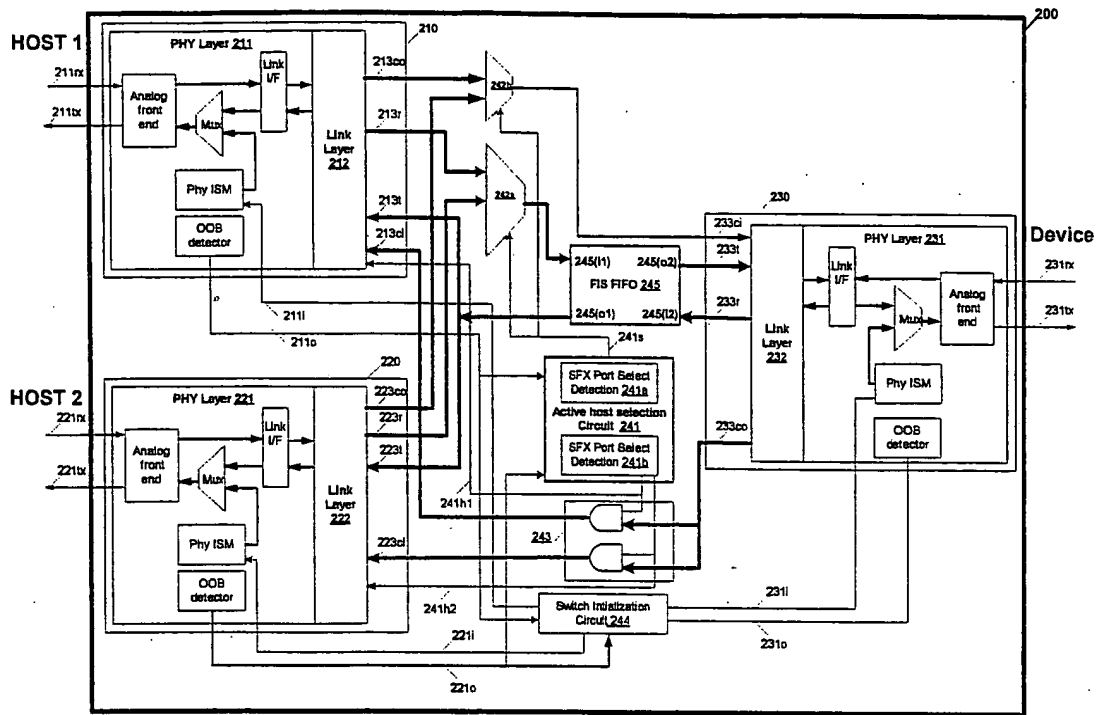


Fig. 5

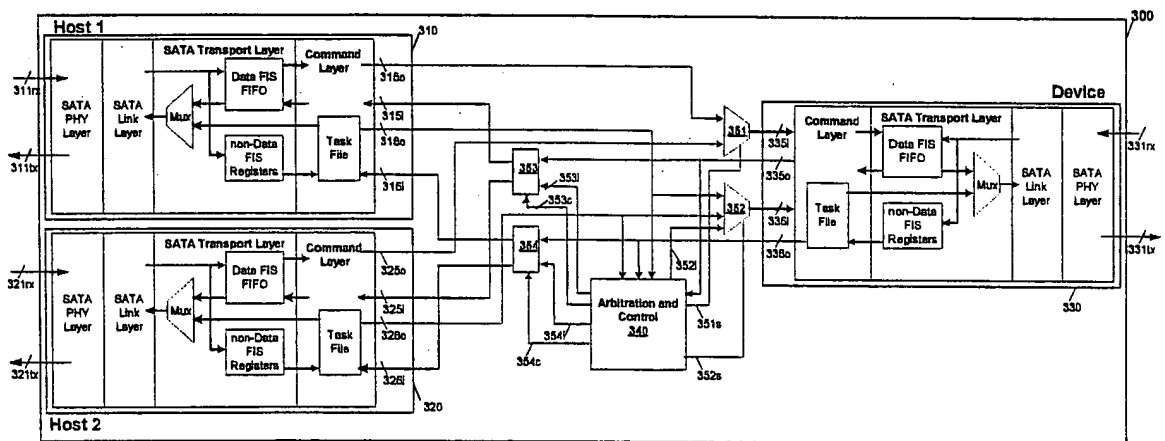


Fig. 6

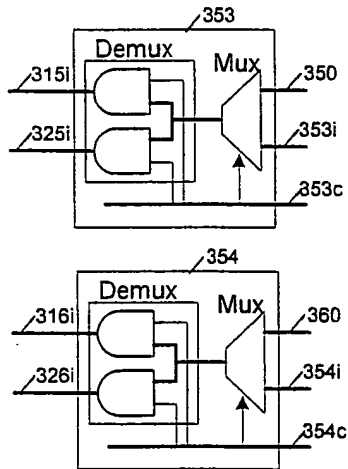


Fig. 7c

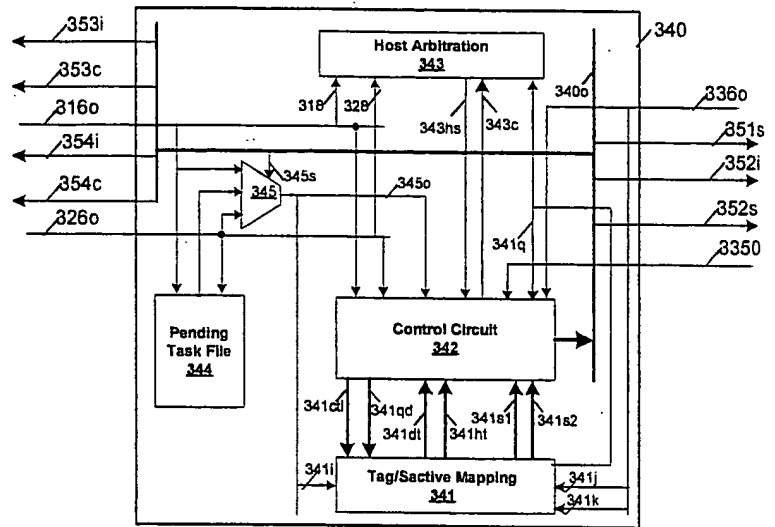


Fig. 7a

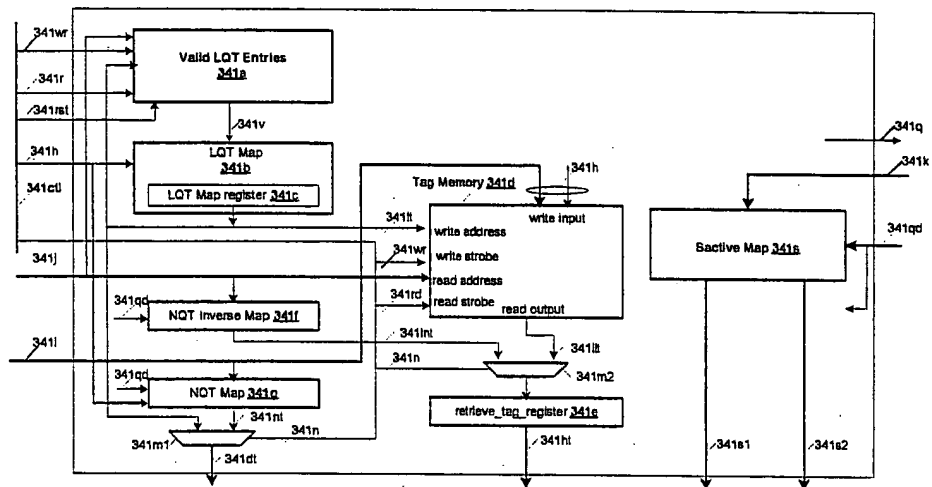


Fig. 7b

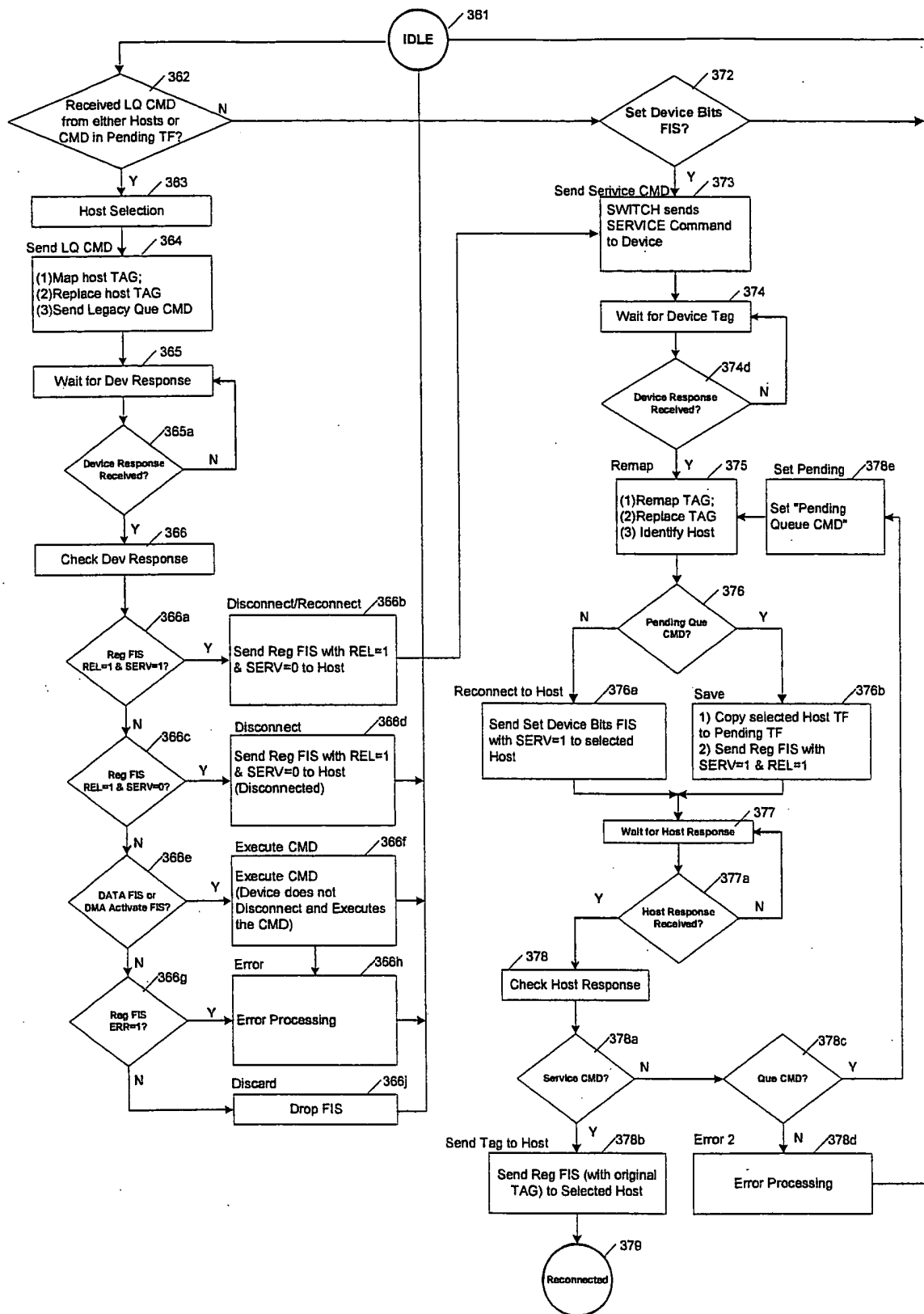


Fig 8a

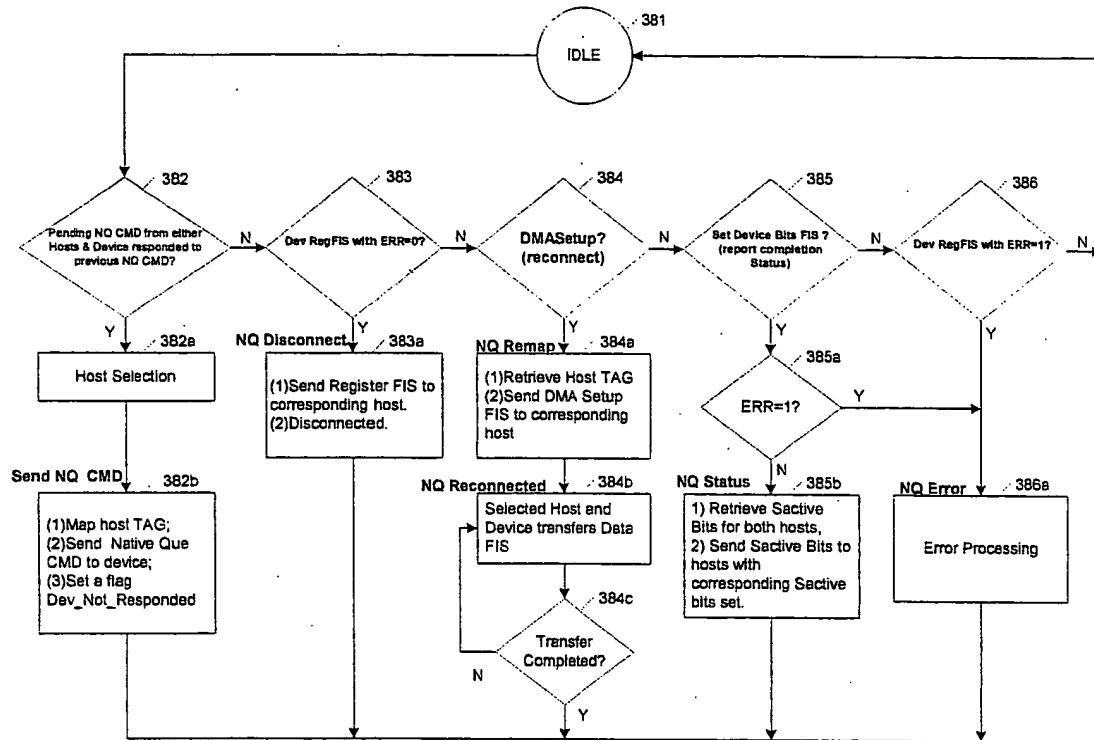


Fig 8b

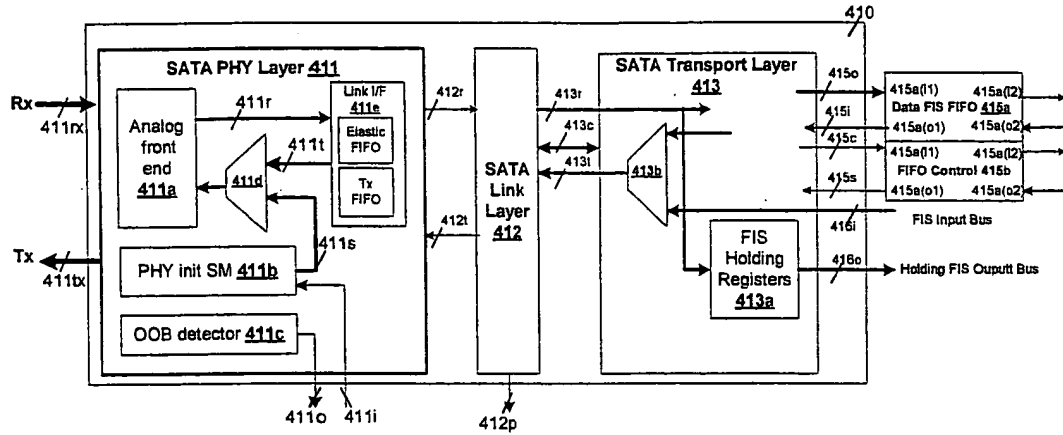


Fig. 9

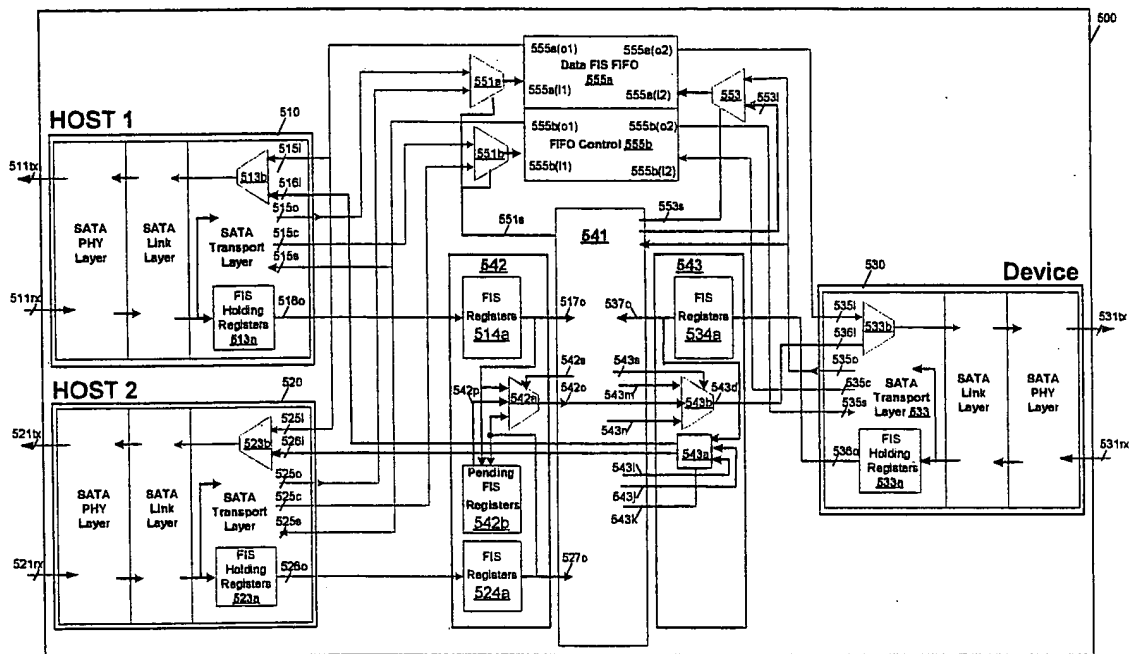


Fig. 10a

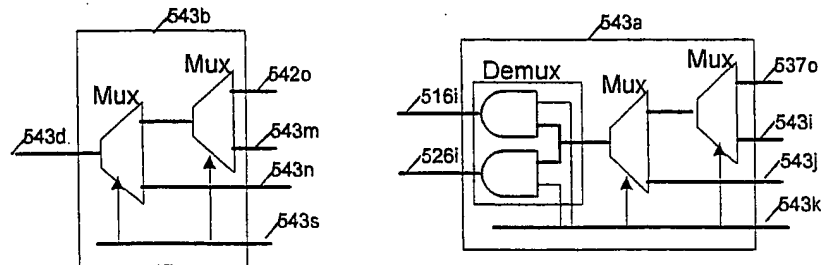


Fig. 10c

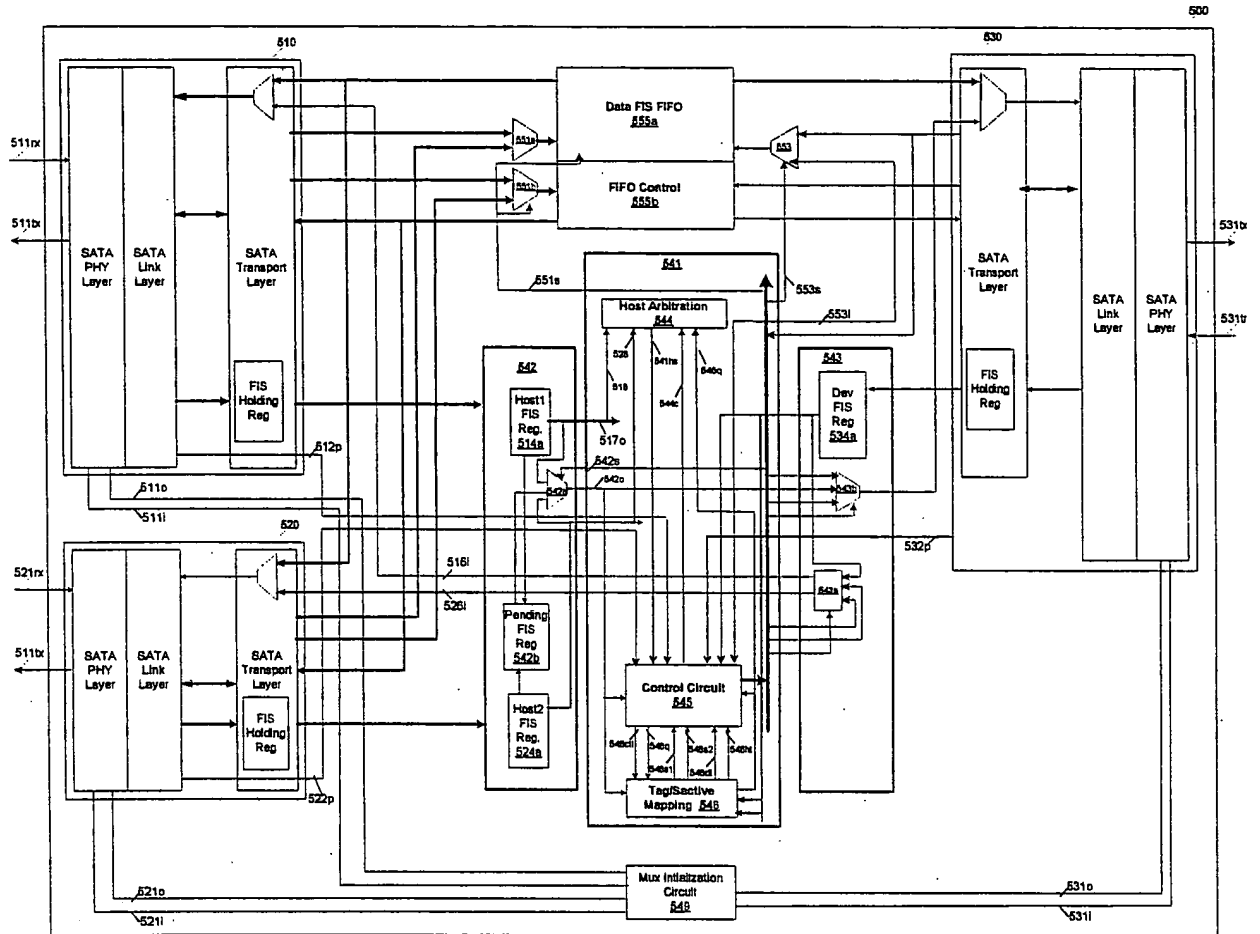


Fig. 10b

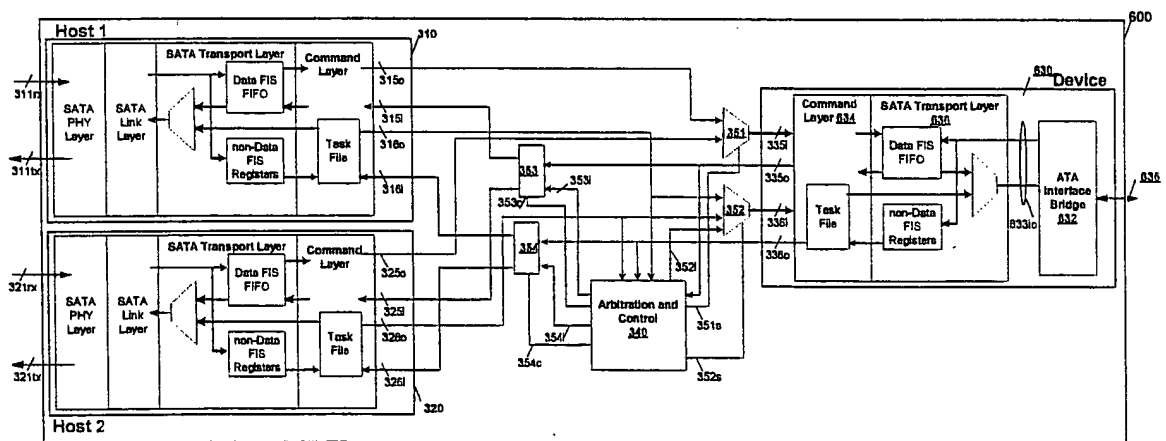


Fig. 11a

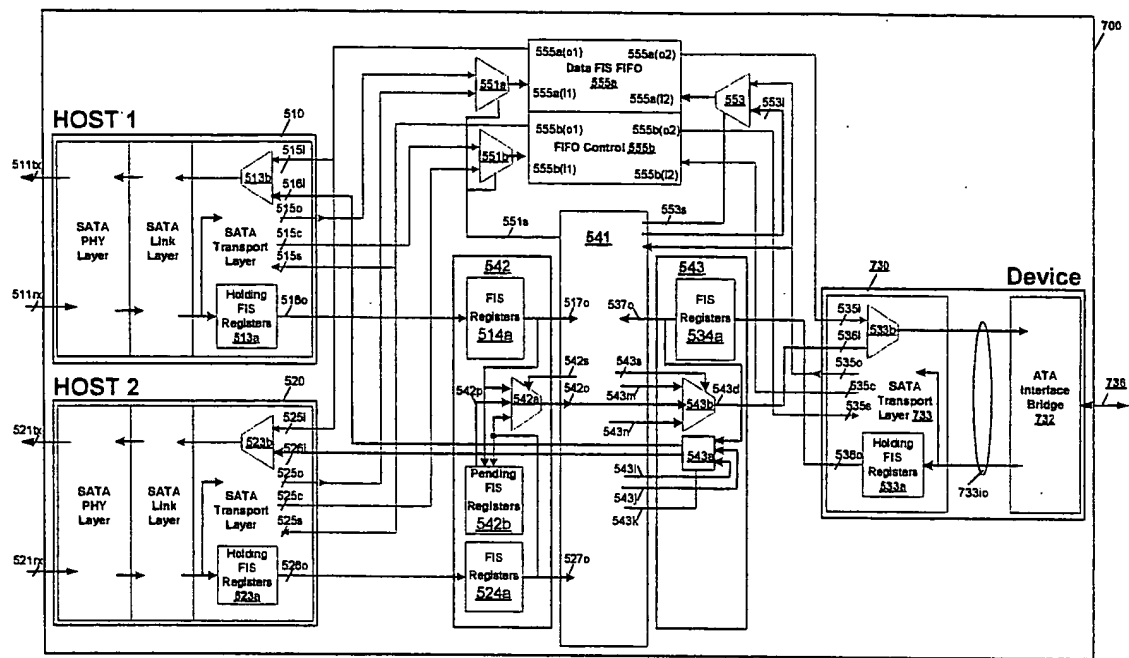


Fig. 11b

90(i)

H-blt 191 (11)

90(ii)

H-bit 91 (III)

90(iii)

H-bll ,91(i)

90(vi)

H-blit 91(

90(v)

0	Error	Status	R	I	D	Reserved (0)	FIS Type (5Fh)	90(vi)
1	Dev / Head	Cyl High				Cyl Low	Sector Number	
2	Reserved (0)	Cyl High (exp)				Cyl Low (exp)	Sector Num (exp) (0)	
3	E_Status	Reserved (0)				Sector Count (exp)	Sector Count	
4	Reserved (0)				Transfer Count			

Fig. 12 (vi) PIO Setup FIS

0	Reserved (0)	Reserved (0)	R	R	R	Reserved (0)	FIS Type (46h)	90(vii)
...	N Dwords of data (minimum of one Dword - maximum of 2048 Dwords)							
...								
n								

Fig. 12(vii) Data FIS

0	Reserved (0)	Pattern Definition	R	R	R	Reserved (0)	FIS Type (58h)	90(viii)
		T A S L F P R V						
1	Data [31:24]	Data [23:16]	Data [15:8]		Data [7:0]			
2	Data [31:24]	Data [23:16]	Data [15:8]		Data [7:0]			

Fig. 12 (viii) BIST Activate FIS

Fig. 12